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| EXAMINER | |
|---|---|
| HO, TU TU V | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2818 | |

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/791,750 | TAKASE, KENJI | |
| | Examiner | Art Unit | |
| | Tu-Tu Ho | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *11 and 12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 13-20* is/are rejected.

7)☒ Claim(s) *1,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/04/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Oath/Declaration*

1. The oath/declaration filed on 03/04/2004 is acceptable.

### *Election/ Restriction*

2. Applicant's election without traverse of Invention I, claims 1-10 and13-20 in the reply filed on 07/07/2005 is acknowledged.

3. Claims 11 and 12 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 07/07/2005, as noted above.

### *Drawings*

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: reference character **101a**, Fig. 9. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to

obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "an electrically conductive foil is attached at said end face" of claim 17 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

**6.** **Claim 1** is objected to because of the following informalities: Claim 1 recites: "A semiconductor device in which one or more semiconductor chips have been mounted onto one or more substrates incorporating patterned wiring and the entirety or entireties has or have been sealed with one or more resins". It is not clear the entirety or entireties is that or those of the semiconductor chip(s) or substrate(s). For examination purpose, the limitation the entirety or entireties applied to the semiconductor chip(s).

**Claim 16** is objected to because of the following informalities: Claim 16 recites: "a semiconductor chip mounted on said substrate and having an end face....an electrically conductive shielding pattern is formed at said end face". It is not clear that the end face is that of the semiconductor chip or that of the substrate. For examination purpose, the end face is that of the substrate.

**Claim 17** is objected to because of the following informalities: Claim 17 recites: "a semiconductor chip mounted on said substrate and having an end face....an electrically conductive foil is formed at said end face". It is not clear that the end face is that of the semiconductor chip or that of the substrate. For examination purpose, the end face is that of the substrate.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. **Claim 8** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites: "one or more electrically conductive patterns is or are formed at one or more end faces at the bottom of at least one of the substrate or substrates; and at least as many terminal or terminals of such number, size, and shape as is or are sufficient for connection to the patterned wiring is or are formed by using one or more dies to blank out and shape at least one region at or in the vicinity of at least one of the electrically conductive pattern or patterns". It is not clear as to how the one or more dies blank(s) out and shape(s), and to what shape and to what degree, the at least one region at or in the vicinity of at least one of the electrically conductive pattern or patterns. In addition, the limitation "using one or more die to blank out" appears to carry a product-by-process limitation as the "one or more die to blank out", as best as can be understood, is used in an intermediate step and is not in the final product, and a product-by-process limitation, as is well established, is considered a non-limitation in a device claim.

For examination purposes, the limitation "one or more electrically conductive patterns is or are formed at one or more end faces at the bottom of at least one of the substrate or substrates; and at least as many terminal or terminals of such number, size, and shape as is or are sufficient for connection to the patterned wiring is or are formed by using one or more dies to blank out and shape at least one region at or in the vicinity of at least one of the electrically conductive pattern or patterns" is only considered as "one or more electrically conductive patterns is or are formed at one or more end faces at the bottom of at least one of the substrate or substrates; and at

least as many terminal or terminals of such number, size, and shape as is or are sufficient for connection to the patterned wiring is or are formed".

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**8.** **Claims 1-2, 8, 10, and 16-18** are rejected under 35 U.S.C. 102(b) as being anticipated by Gevins et al. U.S. Patent 5,038,782 (the '782 reference).

The '782 reference discloses in Figure 4 and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 16**, the reference discloses a semiconductor device comprising:

a substrate (34); and

a semiconductor chip (such as 35a) mounted on said substrate, said substrate having an end face (such as a top face and a bottom face) and incorporating patterned wiring (36 or 37) and sealed with a resin ("Velcro" ™, column 6, lines 35-40, and "sealed" is interpreted broadly; and for a disclosure that Velcro is a resin, see, for example Caires U.S. Patent 4,774,638, column 2, lines 59-62);

wherein an electrically conductive shielding pattern (37 or 36, column 5, lines 49-60) is formed at said end face".

Referring to **claim 17** and using the same reference characters, citations, and interpretations as detailed above for claim 16 where applicable, the reference discloses a semiconductor device comprising:

a substrate (34); and

a semiconductor chip (such as 35a) mounted on said substrate, said substrate having an end face (such as a top face and a bottom face) and incorporating patterned wiring and sealed with a resin ("Velcro" ™, column 6, lines 35-40, and "sealed" is interpreted broadly);

wherein an electrically conductive foil (37 or 36, column 5, lines 49-60) is formed at said end face".

Referring to **claim 1** and using the same reference characters, citations, and interpretations as detailed above for claim 16 where applicable, the reference discloses a semiconductor device in which one or more semiconductor chips have been mounted onto one or more substrates incorporating patterned wiring and the entirety or entireties of the one or more semiconductor chips has or have been sealed with one or more resins, wherein:

one or more electrically conductive patterns (37 or 36) for shielding is or are formed at one or more end faces at the top of at least one of the substrate or substrates.

Referring to **claim 8** and using the same reference characters, citations, and interpretations as detailed above for claim 16 where applicable, the reference discloses a semiconductor device in which one or more semiconductor chips have been mounted onto one or more substrates incorporating patterned wiring and the entirety or entireties of the one or more semiconductor chips has or have been sealed with one or more resins, wherein:

one or more electrically conductive patterns (37 or 36) is or are formed at one or more end faces at the bottom of at least one of the substrate or substrates; and

at least as many terminal or terminals (30) of such number, size, and shape as is or are sufficient for connection to the patterned wiring is or are formed.

Referring to **claim 2**, the reference further discloses that at least one of the electrically conductive pattern or patterns (37 or 36) is at least one copper foil pattern (column 5, lines 49-60).

Referring to **claim 18**, the reference further discloses that said electrically conductive foil (37 or 36) comprises copper (column 5, lines 49-60).

Referring to **claim 10**, the reference further discloses that at least one gold plating is applied to at least one end face of at least one of the terminal or terminals (30, column 5, lines 25-30).

**9. Claims 1, 8-9, and 16-17** are rejected under 35 U.S.C. 102(b) as being anticipated by Kishita U.S. Patent 5,656,857 (the '857 reference).

The '857 reference discloses in Figure 8 and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 16**, the reference discloses a semiconductor device comprising:

a substrate (11); and

a semiconductor chip (20) mounted on said substrate, said substrate having an end face (such as a top face and a bottom face) and incorporating patterned wiring (18a or 12) and sealed with a resin (24,34);

wherein an electrically conductive shielding pattern (12 or 18a, columns 1 and 2, particularly column 2, lines 29-30) is formed at said end face".

Referring to **claim 17** and using the same reference characters, citations, and interpretations as detailed above for claim 16 where applicable, the reference discloses a semiconductor device comprising:

a substrate; and

a semiconductor chip mounted on said substrate, said substrate having an end face (such as a top face and a bottom face) and incorporating patterned wiring and sealed with a resin ("Velcro" ™, column 6, lines 35-40, and "sealed" is interpreted broadly);

wherein an electrically conductive foil (12 or 18a) is formed at said end face".

Referring to **claim 1** and using the same reference characters, citations, and interpretations as detailed above for claim 16 where applicable, the reference discloses a semiconductor device in which one or more semiconductor chips have been mounted onto one or more substrates incorporating patterned wiring and the entirety or entireties of the one or more semiconductor chips has or have been sealed with one or more resins, wherein:

one or more electrically conductive patterns (12 or 18a, columns 1 and 2, particularly column 2, lines 29-30) for shielding is or are formed at one or more end faces at the top of at least one of the substrate or substrates.

Referring to **claim 8** and using the same reference characters, citations, and interpretations as detailed above for claim 16 where applicable, the reference discloses a semiconductor device in which one or more semiconductor chips have been mounted onto one or

more substrates incorporating patterned wiring and the entirety or entireties of the one or more semiconductor chips has or have been sealed with one or more resins, wherein:

one or more electrically conductive patterns (12 or 18a, columns 1 and 2, particularly column 2, lines 29-30) is or are formed at one or more end faces at the bottom of at least one of the substrate or substrates; and

at least as many terminal or terminals (such as 33a or 17) of such number, size, and shape as is or are sufficient for connection to the patterned wiring is or are formed.

Referring to **claim 9**, the reference further discloses that at least one of the terminal or terminals (33a) is formed so as to at least partially protrude to the exterior and so as to have at least one more or less rectangular cross-section.

**10. Claims 1-2, 8, 10, and 16-18** are rejected under 35 U.S.C. 102(b) as being anticipated by Juso et al. U.S. Patent Application Publication 20020000327 (the '327 reference).

The '327 reference discloses in the figures, particularly Figures 16's, 1, and 19, and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 16**, the reference discloses a semiconductor device comprising:

a substrate (1, Fig. 16's, 1, and 19); and

a semiconductor chip (2) mounted on said substrate, said substrate having an end face (such as a top face and a bottom face) and incorporating patterned wiring (4 or 4') and sealed with a resin (11);

wherein an electrically conductive shielding pattern (4' or 4) is formed at said end face".

Referring to **claim 17** and using the same reference characters, citations, and interpretations as detailed above for claim 16 where applicable, the reference discloses a semiconductor device comprising:

a substrate (1); and

a semiconductor chip (2) mounted on said substrate, said substrate having an end face (such as a top face and a bottom face) and incorporating patterned wiring (4 or 4') and sealed with a resin;

wherein an electrically conductive foil (4', 4, or 20, Fig. 1 and 16(b)) is formed at said end face".

Referring to **claim 1** and using the same reference characters, citations, and interpretations as detailed above for claim 16 where applicable, the reference discloses a semiconductor device in which one or more semiconductor chips have been mounted onto one or more substrates incorporating patterned wiring and the entirety or entireties of the one or more semiconductor chips has or have been sealed with one or more resins, wherein:

one or more electrically conductive patterns (4', 4, or 20, Fig. 1 and 16(b)) for shielding (paragraph [0149], and note that, for the record, although the reference only explicitly teaches that copper foil 20 is for shielding, copper foil pattern 4 and 4' also inherently possess shielding property, similar to the present invention) is or are formed at one or more end faces at the top of at least one of the substrate or substrates.

Referring to **claim 8** and using the same reference characters, citations, and interpretations as detailed above for claims 16 and 1 where applicable, the reference discloses a semiconductor device in which one or more semiconductor chips have been mounted onto one or more substrates incorporating patterned wiring and the entirety or entireties of the one or more semiconductor chips has or have been sealed with one or more resins, wherein:

one or more electrically conductive patterns (4', 4, or 20, Fig. 1 and 16(b)) is or are formed at one or more end faces at the bottom of at least one of the substrate or substrates; and

at least as many terminal or terminals (5) of such number, size, and shape as is or are sufficient for connection to the patterned wiring is or are formed.

Referring to **claim 2**, the reference further discloses that at least one of the electrically conductive pattern or patterns (4', 4, or 20, Fig. 1 and 16(b)) is at least one copper foil pattern (paragraphs [0085] and [0149]).

Referring to **claim 18**, the reference further discloses that said electrically conductive foil (4', 4, or 20, Fig. 1 and 16(b)) comprises copper (paragraphs [0085] and [0149]).

Referring to **claim 10**, the reference further discloses that at least one gold plating is applied to at least one end face of at least one of the terminal or terminals (paragraph [0084]).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**11.** **Claims 3-4 and 19-20** are rejected under 35 U.S.C. §103(a) as being unpatentable over Gevins et al. U.S. Patent 5,038,782 (the '782 reference) as applied to claims 2 and 18 above, and further in view of knowledge in the art as disclosed by McKaveney U.S. Patent 4,447,492.

The '782 reference discloses a semiconductor device substantially as claimed and as detailed above including the copper foil or the least one of the copper foil pattern or patterns, but

fails to teach that a gold plating is applied over the copper foil or at least the least one of the copper foil pattern or patterns.

However, as is known, copper is prone to oxidation which increases resistance, and it has been customary to plate copper with gold, to prevent oxidation of copper (see, for example, McKaveney, column 1, lines 45-64).

Therefore, it would have been obvious to form the copper foil or the least one of the copper foil pattern or patterns of the '782 reference such that the copper foil or the least one of the copper foil pattern or patterns include(s) a gold plating. One would have been motivated to make such a change in view of knowledge in the art, as disclosed by McKaveney, as an example, that such a plating of gold prevents oxidation of coper foil.

**12.** **Claims 3-4 and 19-20** are rejected under 35 U.S.C. §103(a) as being unpatentable over Juso et al. U.S. Patent Application Publication 20020000327 (the '327 reference) as applied to claims 2 and 18 above, and further in view of knowledge in the art as disclosed by McKaveney U.S. Patent 4,447,492.

The '327 reference discloses a semiconductor device substantially as claimed and as detailed above including the copper foil or the least one of the copper foil pattern or patterns, but fails to teach that a gold plating is applied over the copper foil or at least the least one of the copper foil pattern or patterns.

However, as is known, copper is prone to oxidation which increases resistance, and it has been customary to plate copper with gold, to prevent oxidation of copper (see, for example, McKaveney, column 1, lines 45-64).

Therefore, it would have been obvious to form the copper foil or the least one of the copper foil pattern or patterns of the '327 reference such that the copper foil or the least one of the copper foil pattern or patterns include(s) a gold plating. One would have been motivated to make such a change in view of knowledge in the art, as disclosed by McKaveney, as an example, that such a plating of gold prevents oxidation of the coper foil.

13. **Claims 1-3, 5, 7-10 and 13-19** are rejected under 35 U.S.C. §103(a) as being unpatentable over admitted prior art (APA, Figs 7-9) in view of Inoue et al. U.S. Patent 5,270,493.

APA discloses a semiconductor device substantially as claimed including IC chips that are susceptible to magnetic noise (present invention, paragraph [0007]) and formed on a substrate carrier, but fails to teach an adequate shielding as claimed. Specifically, the APA fails to disclose a copper foil or copper foil pattern or patterns at an end face of the substrate carrier as claimed.

Inoue, in disclosing a substrate carrier (a printed circuit board) for semiconductor devices, teaches that a copper foil or copper foil pattern or patterns at an end face of the substrate carrier provides excellent electromagnetic shield effect (columns 4 and 12, particularly column 4, first paragraph and column 12, last paragraph).

Therefore, it would have been obvious to form the APA's device such that it includes a copper foil or copper foil pattern or patterns at an end face of the substrate carrier. One would have been motivated to make such a change in view of the teachings in Inoue that such a change provides excellent electromagnetic shield effect.

Referring to **claim 10**, Inoue further teaches that at least one gold plating is applied to at least one end face of at least one of the terminal or terminals (column 6, lines 15-23)

**14.** **Claims 4, 6, and 20** are rejected under 35 U.S.C. §103(a) as being unpatentable over admitted prior art (APA, Figs 7-9) in view of Inoue et al. U.S. Patent 5,270,493 as applied above for claims 1-3, 5, 7-10 and 13-19, and further in view of knowledge in the art as disclosed by McKaveney U.S. Patent 4,447,492.

The APA device modified in view of Inoue is a semiconductor device including the copper foil or the least one of the copper foil pattern or patterns, but fails to teach that a gold plating is applied over the copper foil or at least the least one of the copper foil pattern or patterns.

However, as is known, copper is prone to oxidation which increases resistance, and it has been customary to plate copper with gold, to prevent oxidation of copper (see, for example, McKaveney, column 1, lines 45-64).

Therefore, it would have been obvious to form the copper foil or the least one of the copper foil pattern or patterns of the APA device modified in view of Inoue such that the copper foil or the least one of the copper foil pattern or patterns include(s) a gold plating. One would have been motivated to make such a change in view of knowledge in the art, as disclosed by McKaveney, as an example, that such a plating of gold prevents oxidation of the coper foil.

**15. Claims 1-3, 5, 7-10 and 13-19** are rejected under 35 U.S.C. §103(a) as being unpatentable over Horio et al. U.S. Patent 6,590,152 (the '152 reference) in view of Inoue et al. U.S. Patent 5,270,493.

Similarly to APA, the '152 reference discloses a semiconductor device substantially as claimed including IC chips (2A, 2B, 2C, Fig.4) that are susceptible to magnetic noise (the '152 reference, column 1, lines 15-20) and formed on a substrate carrier (10) including conductive pattern (12) and terminals (12b, Fig. 5), but fails to teach an adequate shielding as claimed. Specifically, the '152 reference fails to disclose a copper foil or copper foil pattern or patterns at an end face of the substrate carrier as claimed.

Inoue, in disclosing a substrate carrier (a printed circuit board) for semiconductor devices, teaches that a copper foil or copper foil pattern or patterns at an end face of the substrate carrier provides excellent electromagnetic shield effect (columns 4 and 12, particularly column 4, first paragraph and column 12, last paragraph).

Therefore, it would have been obvious to form the '152 reference's device such that it includes a copper foil or copper foil pattern or patterns at an end face of the substrate carrier. One would have been motivated to make such a change in view of the teachings in Inoue that such a change provides excellent electromagnetic shield effect.

Referring to **claim 10**, Inoue further teaches that at least one gold plating is applied to at least one end face of at least one of the terminal or terminals (column 6, lines 15-23)

Referring to **claims 7 and 15**, because the '152 reference discloses that a silver is not necessary (column 8, lines 10-20), a silver paste could be used.

16. **Claims 4, 6, and 20** are rejected under 35 U.S.C. §103(a) as being unpatentable over Horio et al. U.S. Patent 6,590,152 (the '152 reference) in view of Inoue et al. U.S. Patent 5,270,493 as applied above for claims 1-3, 5, 7-10 and 13-19 and further in view of knowledge in the art as disclosed by McKaveney U.S. Patent 4,447,492.

The '152 reference's device modified in view of Inoue is a semiconductor device including the copper foil or the least one of the copper foil pattern or patterns, but fails to teach that a gold plating is applied over the copper foil or at least the least one of the copper foil pattern or patterns.

However, as is known, copper is prone to oxidation which increases resistance, and it has been customary to plate copper with gold, to prevent oxidation of copper (see, for example, McKaveney, column 1, lines 45-64).

Therefore, it would have been obvious to form the copper foil or the least one of the copper foil pattern or patterns of the '152 reference's device modified in view of Inoue such that the copper foil or the least one of the copper foil pattern or patterns include(s) a gold plating. One would have been motivated to make such a change in view of knowledge in the art, as disclosed by McKaveney, as an example, that such a plating of gold prevents oxidation of the coper foil.

***Conclusion***

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
July 22, 2005